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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TUNG, KEE M	

ART UNIT	PAPER NUMBER
2671	

DATE MAILED: 10/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/776,439	JEDDELOH, JOSEPH	
	Examiner	Art Unit	
	Kee M. Tung	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The RCE and amendment filed 8/2/05 have been considered in preparing this Office action.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 4-12, 14-16, 18-26 and 28-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horan et al (5,914,727 hereinafter "Horan") in view of Arimilli et al (5,860,101 hereinafter "Arimilli") and Nishida (4,718,006).

As per claim 1, Horan teaches a computer system comprising: a first of the at least two memory controllers (Fig. 3 and c. 11 ll. 5-18: core logic chipset 204 functionally comprises memory interface and control 304) is directly connected to a central processing unit bus, a bus supporting a peripheral device, and the main memory (Fig. 2 and c. 10 ll. 47-54: core logic chipset 204 connected to the host bus 103, PCI bus 109, and memory bus 105), and also wherein the first of the at least two memory controllers comprises an accelerated graphics port for establishing a dedicated point-to-point connection between the first of the at least two memory controllers and an accelerated graphics processor (Fig. 2 and c. 10 ll. 50-51: core logic chipset 204 connected to the graphics controller through an AGP bus 207). Horan discloses that

multiple CPUs in a symmetric or asymmetric multi-processor configuration are contemplated and within the scope of the present invention (c. 10 ll. 45-46 and c. 11 ll. 16-18), but does not expressly teach at least two memory controllers for controlling a main memory. Arimilli teaches a symmetric multiprocessor system comprising multiple partial system memories 18a-18n and corresponding memory controllers 17a-17n (Fig. 2 and c. 6 ll. 18-22) providing the benefit of scalability and parallel bus traffic between the memory controller and system memory. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combined the teachings of Horan and Arimilli whereby the symmetric multiprocessor system contemplated by Horan is implemented with multiple memory controllers and associated system memory as taught by Arimilli in order to provide the benefits of scalability and parallel bus traffic between the memory controller and system memory. However, the combined system still fails to teach or suggest the first of the at least two memory controllers is configured to reroute requests for the other addresses to a second of the at least two memory controllers. This is what Nishida teaches (col. 4, lines 9-18, one of the MCU (such as, MCU1) reroute requests for other addresses to a 2nd (MCU2) of the at least 2 memory controllers). Nishida teaches a data processor system (Figs. 1B and 1C) comprising a plurality of multiprocessor systems (systems 1 and 2), and each multiprocessor system is connected through each memory control unit (MCU0 and MCU1) of each multiprocessor system at least one CPU, and at least one main memory unit (MSUs). Therefore, It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of Nishida into the combined

system of Horan and Arimilli in order to improve access control routes in the memory control unit, thereby improving data throughput in the data processor system as taught by Nishida (col. 2, lines 49-53). Therefore, at least claim 1 would have been obvious.

As per claim 2, Horan discloses: wherein the first of the at least two memory controllers defines a range of addresses in memory that are preferentially used over other addresses for storage of graphics data for transactions associated with the dedicated point-to-point connection (c. 18 ll. 65-c. 19 ll. 4 and Figs. 16 and 17A: chipset configuration registers implemented in the host to PCI bridge function, including register 1702; A Base Address Register 0, BAR0, is used to allocate AGP device address space for the AGP compliant master).

As per claim 4, Horan discloses: wherein the first of the at least two memory controllers maintains a graphical address remapping table comprising at least one page table entry (PTE) providing information for translation of a virtual address to a physical address (c. 9 ll. 51-59: The core logic chipset utilizes a graphics address remapping table to remap virtual addresses to physical addresses of graphics information located in the system memory), wherein the virtual address includes a first portion and a second portion (Fig. 7: graphics controller device address comprising page offset from AGP base address portion and offset into 4KB page portion), the first portion corresponding to a PTE in the graphical address remapping table (Fig. 9: page offset from AGP base address corresponding to address of GART entry) and wherein the second portion and information provided by the PTE are combined to provide the physical address (Fig. 9:

offset into 4KB page portion of the graphics controller device address combined with address of GART entry yields the physical address).

As per claim 5, Horan discloses, wherein the first portion comprises a virtual page number field (Fig. 9: page offset from AGP base address).

As per claim 6, Horan discloses, wherein the second portion comprises an offset field (Fig. 9: offset into 4KB page).

As per claim 7, Horan discloses wherein the graphical address remapping table is configured by loading at least one configuration register during boot up of a computer system (c. 27 ll. 1-5 and ll. 30-35: During boot, system BIOS power-on self-test configures the core logic chipset with size of AGP device address space).

As per claim 8, Horan discloses additionally comprising one configuration register includes a starting address of the graphical address remapping table (c. 22 ll. 16-18: A GART Table/Directory Base Address Register 1910 provides the physical address for the GART table/directory in system memory).

As per claim 9, Horan discloses wherein the at least one configuration register includes a boundary address defining the lowest address of a graphical address remapping table range (c. 22 ll. 16-18: GART Table/Directory Base Address Register 1910 provides the physical address for the GART table/directory in system memory).

As per claim 10, Horan discloses wherein the at least one configuration register includes a range register defining the amount of memory that is preferentially used over other addresses for storage of graphics data for accelerated graphic port transactions

(c. 21 ll. 42-44: An AGP Device Address Space Size Register 1828 determines the size of AGP Device Address Space to be allocated by system BIOS).

As per claim 11, Horan discloses wherein an initialization BIOS loads the at least one configuration register (c. 27 ll. 1-5 and ll. 30-35: During boot, system BIOS power-on self-test configures the core logic chipset with size of AGP device address space).

As per claim 12, Horan discloses wherein an operating system API loads the at least one configuration register (c. 26 ll. 57-59: Key components of the AGP software architecture include System BIOS, the chipset miniport driver, the operating system, and the graphics or Direct Draw driver. These components are required to initialize and control the AGP and GART table functions within the chipset and graphics controller).

Claims 14, 15, and 18-26 are similar in scope to claims 1, 2, and 4-12, and are rejected under the same rationale.

As per claim 16, Horan does not expressly teach at least two of the at least two memory controllers include an accelerated graphics port. Horan contemplates a symmetric or asymmetric multi-processor configuration as within the scope of his invention (c. 10 ll. 45-46 and c. 11 ll. 16-18), and Arimilli teaches a symmetric multiprocessor system comprising multiple partial system memories 18a-18n and corresponding memory controllers 17a-17n (Fig. 2 and c. 6 ll. 18-22). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combined the teachings of Horan and Arimilli whereby the symmetric multiprocessor system contemplated by Horan is implemented with multiple memory controllers and associated system memory as taught by Arimilli wherein at least two of the memory

controllers are connected to respective graphics controllers through respective AGPs in order to provide the benefits of scalability and parallel bus traffic between the memory controller and system memory on behalf of the graphics controllers.

Claims 28-39 and 40-49 are similar in scope to claims 1, 2, and 4-12, and are rejected under the same rationale.

3. Claims 3 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horan et al (5,914,727 hereinafter "Horan") in view of Arimilli et al (5,860,101 hereinafter "Arimilli"), Nishida (4,718,006) and Dye (6,002,411).

As per claims 3 and 17, the teachings of Horan, Arimilli and Nishida are given in previous paragraph of this Office action. However, the combined system fails to expressly teach that at least two of the at least two memory controllers are manufactured on the same chip. Dye teaches an integrated memory controller comprising a single chip and including two memory control units for providing interface signals to communicate with respective banks of the system memory (c. 12 ll. 44-45 and c. 16 ll. 45-47). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Horan, Arimilli, Nishida and Dye, whereby, Horan's chipset is implemented to integrate plural memory controllers as taught by Dye in order to provide faster memory accesses through integration.

4. Claims 13 and 27 rejected under 35 U.S.C. 103(a) as being unpatentable over Horan et al (5,914,727 hereinafter "Horan") in view of Arimilli et al (5,860,101 hereinafter "Arimilli"), Nishida (4,718,006) and Margulis (6,118,462).

As per claims 13 and 27, the teachings of Horan, Arimilli and Nishida are given in previous paragraph of this Office action. However, the combined system fails to expressly teach that one of the at least two memory controllers and a memory are on a single semiconductor chip. Margulis teaches an enhanced system controller 310 connected to an input/output bridge 312, display output devices 330, a PCI bus 332, an accelerated graphics port (AGP) 334, a high-speed serial I/O port 336 (c. 4 ll. 16-19). Integrated into the enhanced system controller are additional internal memory subsystems, each with their own control and data channels (c. 4 ll. 19-21). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Horan, Arimilli, Nishida and Margulis, and to have integrated memory with the memory controller on the chipset in order to improve memory accesses through integration.

5. Claim 50 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horan et al (5,914,727 hereinafter "Horan") in view of Arimilli et al (5,860,101 hereinafter "Arimilli"), Nishida (4,718,006), Margulis (6,118,462) and Dye (6,002,411).

As per claim 50, the teachings of Horan, Arimilli and Nishida are given in previous paragraph of this Office action. However, the combined system fails to expressly teach manufacturing said at least two memory controllers and a memory on a

single semiconductor chip. Margulis teaches an enhanced system controller 310 connected to an input/output bridge 312, display output devices 330, a PCI bus 332, an accelerated graphics port (AGP) 334, a high-speed serial I/O port 336 (c. 4 ll. 16-19). Integrated into the enhanced system controller are additional internal memory subsystems, each with their own control and data channels (c. 4 ll. 19-21). Dye teaches an integrated memory controller comprising a single chip and including two memory control units for providing interface signals to communicate with respective banks of the system memory (c. 12 ll. 44-45 and c. 16 ll. 45-47). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Horan, Arimilli, Nishida, Margulis, and Dye, whereby, Horan's chipset is implemented to integrate plural memory controllers and memory as taught by Margulis and Dye in order to provide faster memory accesses through integration.

Response to Arguments

6. Applicant's arguments filed 8/2/05 have been fully considered but they are not persuasive.

The rejections have been modified in order to fully consider applicant's amendment and response.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kee M. Tung whose telephone number is 571-272-7794. The examiner can normally be reached on Tuesday - Friday from 5:30 am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kee M Tung
Primary Examiner
Art Unit 2671